Virtual Platform for Embedded System Power Estimation

Santhosh Kumar Rethinagiri, Rabie Ben Atitallah, Jean-Luc Dekeyser

Virtual Platform for Embedded System Power Estimation

Santhosh Kumar RETHINAGIRI*, Rabie Ben ATITALLAH† and Jean-Luc DEKEYSER*
*INRIA Lille Nord Europe, Université de Lille1 , France
Email: santhosh-kumar.rethinagiri@inria.fr and jean-luc.dekeyser@inria.fr
†LAMIH, Université de Valenciennes et du Hainaut Cambrésis, Valenciennes, France
Email: rabie.benatitallah@univ-valenciennes.fr

***Abstract*—In this paper, we propose a virtual platform for power estimation of processor based embedded systems. Our platform consists of a combination of Functional Level Power Analysis (FLPA) for power modeling and fast system prototyping for transactional simulation. In this proposal, we aim at estimating power automatically with the help of power models and SystemC IP libraries. These libraries are enriched with different power models and various hardware components required by the embedded platforms. This will allow to use our proposed virtual platform to port various hardware systems and applications in the same environment in order to satisfy the requirements of reliable and efficient design space exploration. Our experiments performed on this virtual embedded platform show that the obtained power estimation results are less than 3% of error in an average for all the processor when compared to the real board measurements.**

I. Introduction

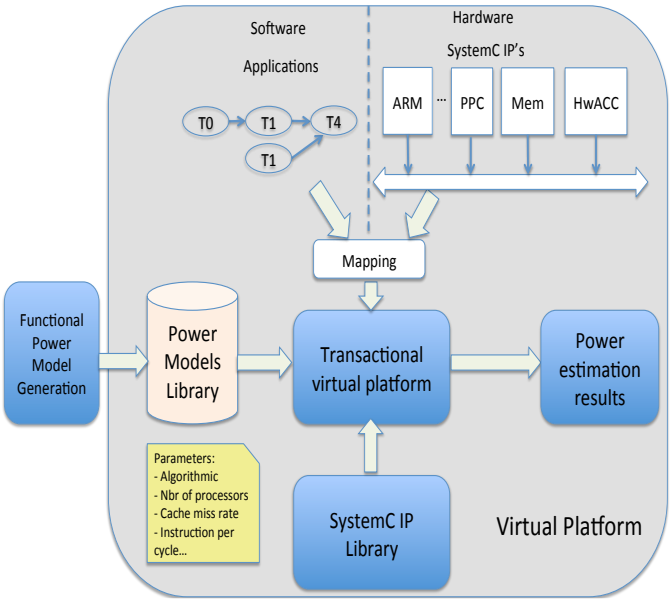

Fig. 1. Proposed virtual platform flow for power estimation

Nowadays, embedded applications are becoming more complex and more resource demanding. For this reason, embedded designers are directed to move towards parallel and symmetric embedded architectures in order to deal with the potential parallelism inherited by the applications. Recently, the ITRS [1] and HiPEAC [1] roadmaps promote power defines performance and power is the wall. In fact, power is becoming one of the two critical pre-design metric factors along with the complexity of embedded systems such as MPSoC, ASIC. Facing this issue, designers should calculate and optimize the power consumption as early as possible in the design flow to reduce the time-to-market and the development cost. In current industrial and academic practices, power estimation using low-level CAD tools is still widely adopted. These low level power estimation tools are however inconvenient to manage the architecture of nowadays complex embedded systems. System-level power estimation using virtual platform is considered as a vital premise to cope with the critical design constraints. However, this objective is tackled by a set of challenges such as, the efficient power modeling and the accuracy in the power estimation.

The keywords in our contribution are hybridization and correlation between abstraction levels. The hybridization is applied here at 2 levels: granularity of activities used to develop the power models in one side and the level of the considered abstraction in the other side. Almost of all the studies focus on power estimation for a given abstraction level without overcoming the wall of speed/accuracy trade-off, the idea is to build up hybrid power estimation virtual platform that gathers different abstraction levels of the system to grab the strict relevant data depending on the power estimation process step. Furthermore, most of the embedded system tools use a component based design approach. Thus, designers build their systems by instantiating different hardware and software IPs (Intellectual Property) from existing libraries. The granularity of the used power models should be coherent with the design approach.

II. Virtual Platform for Power Estimation

The structure of virtual platform for the power estimation of embedded system is illustrated in the Fig. 1. The virtual platform is based on two complementary IP models. First, the functional power IP model, which represents the way the system consumption varies with its activities. Second, the transaction level model, which prototypes the system at the transactional level in order to run virtually and to estimate the total power consumption of the system. Those two models are needed to perform power estimation of the applications. The elaboration of the power model of the targeted platform are done in the functional power model generation step as shown in the Fig. 1. The power model elaboration is based on the Function Level Power Analysis (FLPA) methodology [2]. Dur-

[1]http://www.hipeac.net/system/files/hipeacvision.pdf

TABLE I
POWER ESTIMATION VS POWER MEASUREMENTS FOR H264 APPLICATION WITH DIFFERENT PROCESSOR

Processor	Power Estimation (mW)	Power measurement (mW)
PowerPC (100 MHz)	2430	2450
ARM Cortex (120 MHz) A8	331	342
ARM9 (120 MHz)	156	164
PowerPC (100 MHz) (2 homogenous multiprocessor)	3497	3578

TABLE II
POWER ESTIMATION VS POWER MEASUREMENTS FOR ARM CORTEX A8 PROCESSOR AT 120 MHZ

Program	Power Estimation (mW)	Power measurement (mW)	Error (%)
FIR	311	314	0.8
FFT	313	317	1.04
JPEG2000	331	341	2.9
kalman	320	321	0.5
qsort	313	319	1.94
rindael	318	326	2.49
blowfish	312	320	2.55
bwbp	312	333	1.4
bwbs	312	314	0.7

ing this elaboration, potential functional blocks are identified and the power consumption of each block is characterized by physical measurements. An example of the power model for PowerPC processor based FPGA is given in the equation 1. The generated power models have been adapted to system-level design, as the required activities can be obtained from a system-level environment. For example, equation 1 has the cache miss rate (γ) parameter, which can be obtained from the simulation. For a given platform, the generation of power model is done at once. Then mapping step takes into account the architectural parameters (e.g. the frequency, the number of processors, the processor cache configuration, etc.) and the application porting. It also requires the different activity values on which the power models rely. In order to collect accurately the needed activity values, the activity counter are introduced into transaction virtual platform to communicate with the fast SystemC simulator at the TLM level [3]. The combination of the above two components described at different abstraction levels (functional and TLM) leads to a hybrid virtual platform power estimation that gives a better trade-off between accuracy and speed.

$$P(mW) = 6.3F_{bus} + 4.1\gamma + 1599 \quad (1)$$

III. EXPERIMENTAL RESULTS

Actually, our proposed virtual platform automatically performs the power estimation at the system-level. It takes the users configuration (processor, cache, application, etc..,) and computes the power consumption and the execution time for the corresponding processor based embedded system. The estimation process is very fast as it relies on the SystemC TLM simulation of the system. Several targets can be evaluated as long as several power models and SystemC IP's are available in the library. We have demonstrated with ARM Cortex A8 that the number of external accesses and pipeline stall rate, which have a great impact on the final power consumption and execution time. For the ARM9 and PowerPC, only the number of external access rate and operating frequency, are needed.

For the three different kind of processors in our library the power estimation was performed on a multimedia benchmark and was also measured for the same as shown in the Table I. The precision of our proposed virtual platform varies slightly from a processor to the other. For the ARM Cortex A8, the average error is 2% (see Table II). This definitely demonstrates the possibility of performing an accurate power estimation of application at system-level. Another important aspect is energy estimation. Energy estimation is also accurate due to the running the complete program on the virtual platform and by this way, we got an average error of 4%.

IV. CONCLUSION

Our proposed virtual platform for power estimation can perform estimation at the System-Level. We have emphasized the benefits of using different abstraction levels in the context of system-level power estimation tool design. Each level comes with its own characteristics to add the relevant information on the power estimation process. In addition, using functional power models brings transparency regarding the low level implementation, reduces the number of dependent parameters, and eases the extraction of the required data. Our proposed virtual platform explores these two aspects and offers an accurate and fast system-level power estimation. In future works, our investigation will concern the scalability of the system to cover various DSP architectures executed on heterogeneous multiprocessor architectures.

REFERENCES

[1] ITRS. Design, 2010 edition. http://public.itrs.net/, 2010.

[2] J. Laurent, N. Julien, and E. Martin. High level energy estimation for DSP systems. In *Proc. Int. Workshop on Power And Timing Modeling, Optimization and Simulation PATMOS'01*, pages 311–316, 2001.

[3] Open SystemC Initiative. Systemc, 2008. World Wide Web document, URL: http://www.systemc.org/.